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S/N 09/145,595 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ji Ung Lee	Examiner: Karabi Guharay
Serial No.:	09/145,595	Group Art Unit: 2879
Filed:	September 2, 1998	Docket: 303.537US1
Title:	FIELD EMISSION DEVICES HAVING STRUCTURE FOR REDUCED EMITTER TIP TO GATE SPACING	

APPEAL BRIEF TO THE BOARD OF PATENT APPEALS AND INTERFERENCES OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOX AF
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Appellant's Brief on Appeal

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences filed on July 26, 2002, from the Final Rejection of claims 36-60 of the above-identified application, as set forth in the Final Office Action mailed March 26, 2002.

This Appeal Brief is filed in triplicate and accompanied by the requisite fee set forth in 37 C.F.R. § 1.17(c). Applicant respectfully requests reversal of the Examiner's rejection of pending claims 36-60.

APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Micron Technology, Inc., a Delaware corporation doing business at 8000 South Federal Way, P.O. Box 6, Boise, Idaho 83707-0006.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to the Applicant which will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 36-60 are pending, and claims 36-60 are the subject of the present appeal (see Appendix 1).

4. STATUS OF AMENDMENTS

This application was originally filed on September 2, 1998, with claims 1-46.

In the first Office Action mailed April 3, 2000, claims 1-35 were canceled, subject to a restriction requirement. Claims 36-46 remained pending, and were rejected under 35 U.S.C. §103(a) as being unpatentable over the single reference of Cloud et al. (U.S. Pat. No. 5,653,619).

In the first Amendment and Response filed June 28, 2000, Appellant responded to the first Office Action amending claims 36 and 43.

In the second Office Action mailed September 1, 2000, claims 36-46 were rejected under 35 U.S.C. §103(a) as being unpatentable over the single reference of Cloud et al. (U.S. Pat. No. 5,653,619).

In the second Amendment and Response mailed November 1, 2000, Appellant responded to the second Office Action without amending claims 36-46.

In the Advisory Action mailed December 5, 2000, the Amendment and Response mailed on November 1, 2000 was not entered in the file, and was indicated as not placing the application in condition for allowance.

In the Continuing Patent Application (CPA) filed December 21, 2000, Appellant requested that the Amendment and Response mailed November 1, 2000 be entered in the file.

In the first and final Office Action mailed February 22, 2001, claims 36-46 were rejected under 35 U.S.C. §103(a) as being unpatentable over the single reference of Cloud et al. (U.S. Pat. No. 5,653,619).

In the first Amendment and Response filed April 23, 2001, Appellant added new claims 47-60, and responded to the first Office Action without amending claims 36-46.

In the Advisory Action mailed 5/14/01, the Amendment and Response mailed on April 23, 2001 was not entered in the file, and was indicated as not placing the application in condition for allowance.

In the Request for Continued Examination (RCE) mailed on May 22, 2001, Appellant requested that the Amendment and Response mailed April 23, 2001 be entered in the file.

In the first Office Action mailed August 15, 2001, claims 47-60 were rejected under 35 U.S.C. §112 and claims 36-60 were rejected under 35 U.S.C. §103(a) as being unpatentable over the single reference of Cloud et al. (U.S. Pat. No. 5,653,619).

In the first Amendment and Response mailed November 15, 2001, Appellant amended claims 46 and 47-60 pursuant to 112 related issues.

In the second Office Action mailed March 26, 2002, claims 36-60 were finally rejected under 35 U.S.C. §103(a) as being unpatentable over the single reference of Cloud et al. (U.S. Pat. No. 5,653,619).

In the second Amendment and Response mailed May 28, 2002, Appellant requested reconsideration and withdrawal of the final 35 U.S.C. §103(a) rejection. The Response was mailed in the form of an Appeal Brief.

In the Advisory Action mailed June 27, 2002, the final rejection of claims 36-60 under 35 U.S.C. §103(a) was maintained.

5. SUMMARY OF THE INVENTION

An illustrative embodiment of the present invention includes a method for forming a self-aligned gate structure around an electron emitting tip. The method includes forming a cathode on a substrate. The cathode includes an emitter tip. An insulator layer is formed over the

cathode and the emitter tip. The insulator is ion etched and a gate is formed on the insulator layer.

In another embodiment, a method of forming a field emission device on a substrate is provided. The method includes forming a cathode emitter tip in a cathode region of the substrate. A gate insulator layer is formed on the emitter tip and the substrate. An ion etch process is used in order to reduce the thickness of the gate insulator layer in the cathode region more rapidly than in the isolation region. Further, the method includes forming a gate on the gate insulator layer and an anode is formed opposing the emitter tip.

In another embodiment, a field emitter array is provided. The field emitter array includes a number of cathodes which are formed in rows along a substrate. A gate insulator is formed along the substrate and surrounds the cathodes. A number of gate lines are formed on the gate insulator. And, a number of anodes are formed in columns orthogonal to and opposing the rows of cathodes. The field emitter array is formed according to a method which includes the following: forming a number of cathode emitter tips in cathode regions of the substrate, forming a gate insulator layer on the emitter tips and the substrate such that forming the gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate, forming a number of gate lines on the gate insulator layer, and forming a number of anodes opposite the emitter tips.

Thus, an improved structure and method are provided which will allow a smaller distance between the emitter tip and the gate structure without having to decrease the thickness of the gate dielectric which increases capacitance. A smaller emitter tip to gate distance lowers the turn-on voltage which is highly desirable in such areas as beam optics and power dissipation. The improved method and structure include the use of an energetic ion etch. Including the etch process removes portions of the sloped surface of a conformally covered emitter tip more rapidly than the flat portions of the gate isolation layer or surface. The method promotes a streamlined fabrication sequence and yields a structure with improved performance.

6. ISSUES PRESENTED FOR REVIEW

A. Whether the drawings of the Cloud reference teach variations in thickness of an insulating layer.

B. Whether the specification of the Cloud reference teaches variations in thickness of an insulating layer that allow a portion of a gate layer to be closer to a cathode than a distance separating the gate layer from a substrate.

7. GROUPING OF CLAIMS

Claims 36-60 are to be considered together for purposes of this appeal. The claims stand or fall together.

8. ARGUMENT

A. The drawings of the Cloud reference do not teach variations in thickness of an insulating layer.

Applicant submits that the drawings of Cloud must be interpreted in light of the specification. The Examiner's rejection from the Office Action of August 15, 2001 states:

> Cloud et al. further disclose that a distance separating the number of cathode emitter tips from the number of gate lines is significantly thinner than a separation distance separating the number of gate lines and the substrate (see Fig 1, Fig 2, and Fig 2B).

Applicant respectfully submits that the drawings must be interpreted in light of the specification. Pursuant to MPEP 2125 "proportions of features in a drawing are not evidence of actual proportions when drawings are not to scale." MPEP 2125 goes on to state that "when the reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurements are of little value. However, the description of the article pictured can be relied on, in combination with the drawings, for what they would reasonably teach one of ordinary skill in the art."

The Cloud reference does not appear to indicate that the drawings are to scale, and the Cloud reference appears to be silent as to dimensions. Therefore, Applicant submits that the superficial appearance alone of Figures 1, 2, 2A and 2B does not support a 103(a) rejection in this matter.

B. The specification of the Cloud reference teaches a preferably conformal layer and does not include a gate layer wherein a portion of the gate layer is closer to a cathode than a distance separating the gate layer from a substrate.

The specification of Cloud does not include variations in insulator layer thickness and Cloud teaches away from varying an insulator layer thickness.

As stated in MPEP 2125, "the description of the article pictured can be relied on, in combination with the drawings, for what they would reasonably teach one of ordinary skill in the art." The specification of the Cloud reference appears to discuss a careful process of choosing a uniform thickness for the **conformal** insulating layer in column 5, lines 42-50.

> The thickness of this first insulating layer 18 will substantially determine **both** the gate 15 to cathode 13 spacing, **as well as** the gate 15 to substrate spacing 11. Hence, the insulating layer 18 must be as thin as possible, since small gate 15 to cathode 13 distances result in lower emitter drive voltages, **at the same time**, the insulating layer 18 must be large enough to prevent the oxide breakdown which occurs if the gate is not adequately spaced from the cathode conductor 12.

Cloud **does not teach *variations* in thickness** of the insulating layer 18. It merely teaches that the single uniform thickness chosen must be chosen with certain performance factors in mind as discussed in the Cloud quotation above. In fact, Cloud teaches away from varying the thickness of the insulating layer 18 as cited by the Examiner when Cloud states that the insulating layer is **preferably** conformal (col. 5, line 62).

A gate layer 15 appears to be deposited over the preferably conformal insulating layer 18. Because the preferably conformal insulating layer is uniform in thickness, and no material has been removed from the insulating layer, the distance separating the gate lines from the substrate is equal to the uniform thickness of the insulating layer. Because the thickness of the insulating

layer is uniform, it is impossible for any portion of the gate layer 15 to be closer to the cathode 13 than the distance separating the gate lines from the substrate.

The Examiner's interpretation of Cloud

On page 8 of the Office Action mailed August 15, 2001, and in the Office Action mailed March 26, 2002, reference is made to a portion of the specification of Cloud. However, the portion relied upon (col. 5, lines 52-55) appears to have been misunderstood. The rejection states:

> Cloud teaches that the insulating layer 18 can be deposited to a level substantially equal to or slightly higher than the level of the cathode tips (Lines 52-55 of column 5). In the case, when it is deposited at the level of cathode tip, thickness of the insulating layer 18 above the cathode tip is zero while the thickness of the insulating layer at other locations has a definite value.

A conformal layer as specifically taught by Cloud, by definition, does not vary in thickness. The misunderstanding of Cloud in the pending Office Action appears to arise where Cloud refers to depositing the insulating layer 18 to a level in comparison to the cathode emitter 13. Cloud refers to a level of the cathode emitter 13. One skilled in the art will recognize this as a distance between the base of the cathode emitter 13 and the tip of the cathode emitter. Cloud also refers to a level of the insulating layer 18. One skilled in the art will recognize this as a thickness of the conformal insulating layer 18 in a region spaced apart from the cathode emitter 13. When Cloud describes depositing the insulating layer 18 to a level equal to the level of the cathode emitter 13, the insulating layer level referred to is understood to be an average of the regions that are spaced apart from the emitter tip 13 itself. In the local region of the cathode emitter, one skilled in the art will recognize that the conformal insulating layer 18 maintains its thickness as it "conforms to the shape of the cathode emitter tip 13" (col. 5, line 64).

Applicant is unable to understand how the word "conformal" as specifically taught in Cloud (col. 5, lines 62 and 64) can be used to describe the proposed interpretation with varied layer thicknesses as hypothesized in the August 15, 2001, and March 26, 2002 Office Actions. One skilled in the art will recognize that deposition methods such as CVD used to form insulating layers 18 are only capable of forming conformal layers. Deposited layers uniformly

coat surface features at the same rate. They do not operate under "flow" mechanisms to fill the lowest surface areas first. Variations in thickness of insulating layers are not taught in Cloud, nor are they obvious without teaching as found in the present application.

In contrast, Applicant's invention includes a field emitter array where the distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate. This configuration is impossible without varying a thickness of the insulating layer as taught in the present application.

9. SUMMARY

Because the Figures 1, 2, 2A and 2B of Cloud cited in the pending Office Action do not appear to be designated as being to scale, and no dimensions appear to be included, the Figures alone do not support a 35 USC § 103(a) rejection. When interpreted in light of the specification of Cloud, a conformal insulator layer is show. The conformal insulator layer makes it impossible for Cloud to show a distance separating the number of cathode emitter tips from the number of gates lines that is significantly thinner than a separation distance separating the number of gate lines and the substrate. Reconsideration and withdrawal of Examiner's 35 USC § 103(a) rejection is respectfully requested.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: BOX AF, Commissioner of Patents, Washington, D.C. 20231, on this 26 day of September, 2000.

Tina Kohout
Name

_____
Signature

APPENDIX I

The Claims on Appeal

36. A field emitter array, comprising:

a number of cathodes formed in rows along a substrate;

a gate insulator formed along the substrate and surrounding the cathodes;

a number of gate lines formed on the gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a gate insulator layer on the emitter tips and the substrate, wherein

forming the gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips, and

wherein a distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate.

37. The field emitter array of claim 36, wherein the number of gate lines and the number of cathodes are formed using a self-aligned technique.

38. The field emitter array of claim 36, wherein the number of cathodes include polysilicon cones.

39. The field emitter array of claim 36, wherein the number of cathodes include metal silicides on the polysilicon cones.

40. The field emitter array of claim 36, wherein the substrate includes glass.

41. The field emitter array of claim 36, wherein the number of gate lines include refractory metals.

42. The field emitter array of claim 36, wherein the number of gate lines include doped polysilicon.

43. A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes formed in rows along the substrate;

a gate insulator formed along the substrate and surrounding the cathodes;

a number of gate lines formed on the gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, wherein the anodes include multiple phosphors, and wherein the intersection of the rows and columns form pixels, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a gate insulator layer on the emitter tips and the substrate, wherein forming the gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips;

wherein a distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate;

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

44. The flat panel display of claim 43, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

45. The flat panel display of claim 43, wherein the number of cathodes include metal silicides on the polysilicon cones.

46. The flat panel display of claim 43, wherein the number of gate lines include refractory metals.

47. A field emitter array, comprising:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes.

48. The field emitter array of claim 47, wherein the number of cathodes include polysilicon cones.

49. The field emitter array of claim 47, wherein the number of gate lines include refractory metals.

50. The field emitter array of claim 47, wherein the number of gate lines include doped polysilicon.

51. A field emitter array, comprising:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes;

wherein the number of cathodes include metal silicides on the polysilicon cones.

52. A field emitter array, comprising:

a number of cathodes in rows along a semiconductor-on-glass substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes.

53. A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness;

a number of anodes located in columns orthogonal to and opposing the rows of cathodes; and

a row decoder and a column decoder each coupled to the field emitter array; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

54. The flat panel display of claim 53, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

55. The flat panel display of claim 53, wherein the number of cathodes include metal silicides on the polysilicon cones.

56. The flat panel display of claim 53, wherein the number of gate lines include refractory metals.

57. A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness;

a number of anodes located in columns orthogonal to and opposing the rows of cathodes, wherein the anodes include multiple phosphors, and wherein the intersection of the rows and columns form pixels; and

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

58. The flat panel display of claim 57, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

59. The flat panel display of claim 57, wherein the number of cathodes include metal silicides on the polysilicon cones.

60. The flat panel display of claim 57, wherein the number of gate lines include refractory metals.